REMARKS

Claims 1-4 were pending in the present application. Claims 3 and 4 have been canceled herein due to restriction. Thus claims 1 and 2 are now pending. The applicants respectfully request reconsideration and allowance of the present application in view of the above amendments and the following remarks.

The applicants note with appreciation the acknowledgement of the claim for priority under section 119 and the notice that all certified copies of the priority documents have been received.

The applicants acknowledge and appreciate receiving a copy of the form PTO-1449 submitted with the Information Disclosure Statement filed on February 3, 2004 on which the Examiner has initialed all listed items.

Claims 1 and 2 stand rejected under 35 USC §102(b) as being allegedly anticipated by Kasuya et al., U.S. Patent Application Publication No. US 2001/0009389 A1 (hereinafter "Kasuya"). The rejection is respectfully traversed.

Applicants first generally note that the present invention includes an outputting circuit that is made to output a low or high logical level on the basis of a relationship between current to be supplied from a current supply circuit to a sixth transistor and a current flowing in the sixth transistor. The current supply circuit is made such that, when the supply of current to first and second input-stage transistor circuits comes to a stop, current to be supplied to one of a fifth and the sixth transistors increases while current to be supplied to the other does not vary. Accordingly, in the present invention, an output is fixed to an arbitrary condition in an area where difficulty is encountered in making a decision on the potential difference between an inverting input terminal and a non-inverting input terminal.

Applicants note that the present invention is based on the characteristic that, in a multi-collector PNP transistor arrangement, when a flow of a collector current from one collector (2) is stopped, a portion of an emitter current from an emitter (31), which makes a current flow in the collector (2), flows into the other collector (3) paired with the collector (2). Consequently, the collector current of the other collector (3) is increased. Although Kasuya describes a multi-collector transistor arrangement and a technique of outputting a signal corresponding to a potential difference between input signals to an inverting input terminal and a non-inverting input terminal. Kasuya, at best, incidentally describes the use of a constant current source in paragraph [0058], which is not shown. Accordingly, the current supply arrangement in Kasuya is not of importance in Kasuya and is not based upon the above described collector-current increasing characteristic. Accordingly, Kasuya fails to disclose, *inter alia*, the claimed current suppy circuit in the manner claimed as required.

It is clear that the circuit arrangement according to the claimed invention significantly differs from the operational amplifier described in Kasuya and further, the claimed arrangment possesses advantages obtainable from such differences as described above. Since Kasuya and the present invention differ in purpose from each other, e.g. an object of the present invention to fix the output logical level to a desired level (stabilize the output behavior) when an input signal voltage gets out of the in-phase input voltage range, whereas the object of Kasuya is to enlarge the output range of an operational amplifier by extending the range of supply voltage (Vcc + 1V to GND -1V), the differences are further highlighted. By appreciating the difference in the problems solved by the present invention and the problems solved in Kasuya, a better understanding in the differences between the claimed invention and the arrangement described in Kasuya is possible.

Accordingly, for at least the reasons set forth hereinabove, a *prima facie* case of anticipation has not properly been established in that the applied reference fails to disclose all the claimed features as required. It is respectfully requested that the rejection of independent claim 1 be reconsidered and withdrawn.

Claim 2, by virtue of depending from independent claim 1, is allowable for at least the reasons set forth hereinabove. It is respectfully requested therefore that the rejection of claim 2 be reconsidered and withdrawn.

In view of the foregoing, the applicants respectfully submit that the present application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,

Robert L Scott, II
Reg. No. 43,102

Posz Law Group, PLC
12040 South Lakes Drive, Suite 101
Reston, VA 20191
Phone 703-707-9110
Fax 703-707-9112
Customer No. 23400